Voltage-Tolerant Monolithic L-Band GaAs SPDT Switch

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ABSTRACT

A monolithic GaAs L-band single-pole double-throw nonreflective (SPDTNR) FET switch has been developed. The switch has shown to be significantly less sensitive to DC ripple when compared to conventional FET switches Also, the switch has the advantage of operating with either positive or negative control voltages Small-signal insertion loss is less than 1.3 dB over a 1 to 2 GHz bandwidth with less than 1.3:1 VSWR in all states Isolation exceeds 35 dB, with a switching current requirement of less than 10 uA. The chip size is 0.97 mm x 1.75 mm x 0.15 mm which permits more than 2100 monolithic switches to be fabricated on a 3-inch GaAs wafer.

INTRODUCTION

Series-shunt FET switches are often used for low frequency applications (DC to 6 GHz) when the rf power handling requirements are small (typically under 33 dBm). FET switches have an advantage over PIN diode switches since FET current requirements are on the order of microamperes and do not require external current drivers. For a conventional series-shunt FET switch, the bias voltages must be negative This paper describes a new switch topology which can operate with either positive or negative bias making it TTL and CMOS compatible while minimizing sensitivity to DC bias ripple.

FET MODEL

To obtain the FET models for the switch design, 600 um gatewidth FET's were rf characterized as three-port devices. A model was then fit to the resulting S-parameters. The gate of a FET creates a Schottky diode which can be modeled as a variable capacitor Cgd in parallel with a variable resistor Rgd (Figure 1). The resistance of the gate finger is modeled as a lumped resistor Rg. Rc is the contact resistance of the drain and source pads. Rds and Cds are the variable drain-to-source channel resistance and capacitance. When the gate is forward biased with respect to the drain and source, Rds, Rgd, Cds, and Cgd take on low resistive and capacitive values, respectively. The value of each element is difficult to determine. However, the net result is that the channel is predominately resistive from drain to source (8 ohms). When the gate is reversed biased with respect to the drain and source, Rgd and Rds become very large while Cgd and Cds are quite small The model thereby reduces to an approximate equivalent of 4 ohms in series with a 0.45 pF capacitor from drain to source.

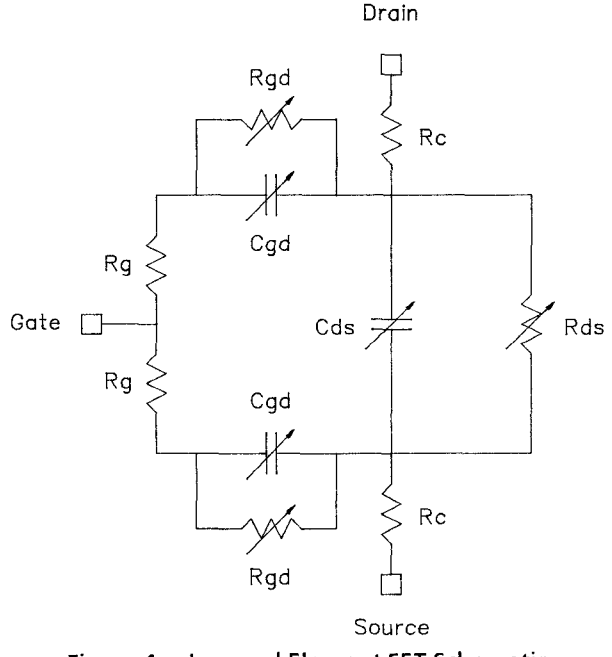


Figure 1. Lumped Element FET Schematic.

MONOLITHIC CIRCUIT DESIGN

A novel approach to reducing bias voltage sensitivity is to DC isolate the switch except for control bias (Figure 2) The shunt FETs are DC blocked, allowing their source potential to float. The 44 pF blocking capacitors are large enough such that their reactance is negligible for the rf frequencies being considered The size of the capacitors is irrelevant to switching speed since the rise time is determined by FET capacitance and bias resistance By applying 4 5 V at VC1, and 0.5 V at VC2, the series FETs in the RF1 path, and the shunt FETs in the RF2 path are forward biased Their gates create a Schottky barrier so that there is a 0 6 V diode drop

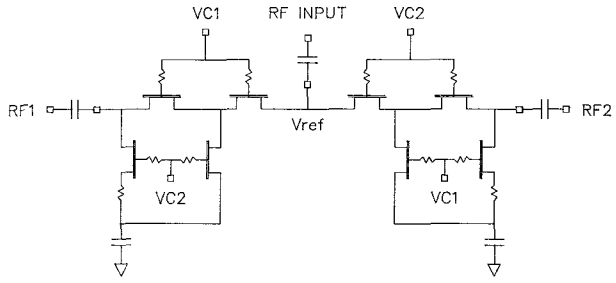


Figure 2. Switch Circuit Schematic.

from gate to drain/source. Thus the voltage potential at Vref is approximately 3.9 V. The shunt FETs in the RF1 path, and the series FETs in the RF2 path are therefore reversed biased by 3.4 V and turned off. The RF1 path is a low insertion loss path, while the RF2 path is isolated. The switch will work equally well with negative bias voltage provided the potential difference is greater than 2.5 V. Nominally the FET drain-source spacing is 0.15 mils. By increasing the drain-source spacing to 0.55 mils in the first shunt FETs, the FET channel on-resistance is approximately 50 ohms and the switch is thereby made nonreflective.

PERFORMANCE

The advantage of this topology over the conventional topology is best seen when comparing insertion loss as a function of VC1 voltage. In the conventional case, as VC1 goes negative the series FET channels become depleted of charge carriers, causing an increase in insertion loss. In the new topology, the series FETs are forward biased so there is no substantial increase in insertion loss until the shunt FETs begin to turn on The turn on point can be expressed as follows:

$$VC2 - Vref = -|Vp|$$

where $Vref = VC1 - 0.6\ V$

and Vp is the pinchoff voltage of the shunt FETs. As an example, with VC2 = -4.5 V, Vp = 1 8 V, no substantial degradation in insertion loss will be detected for the new topology until VC1 becomes less than -2.1 V. Figure 3 shows almost no increase in insertion loss for the new topology for VC1 = -1.25 V whereas in the conventional case, insertion loss increases rapidly.

By holding VC2 constant at -4.5 V and modulating VC1 (at -0.5 V) with a 2 V p-p 125 KHz sinusoidal signal there is a significant reduction in AM modulation of the RF signal for the new topology (Figure 4). In both (a), and (b) the top trace is the -0.5 V at VC1 modulated with a 125 KHz sinusoid. The bottom trace (a) shows a 0.5 dB p-p excursion in the detected rf. The bottom trace (b) shows a 0.1 dB p-p excursion in the detected rf. The rf performance of the switch is summarized in Table 1.

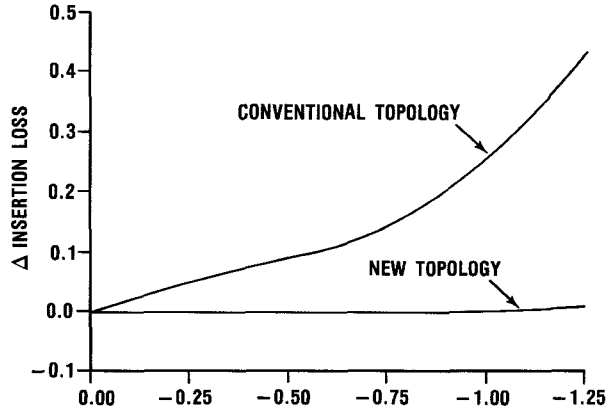
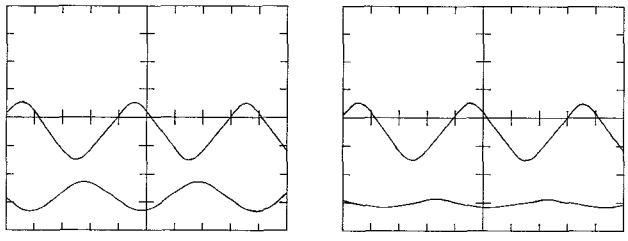


Figure 3. Increasing Insertion Loss As A Function Of Decreasing VC1 Voltage For The RF1 Path (VC2 = -4.5 V)



a) conventional topology b) new topology

Figure 4. Comparison of the AM Modulation for the Detected RF Signal in the New and Old Topology.

Table 1. Switch Performance.

Insertion loss	< 1.3 dB
Isolation	> 35 dB
VSWR	< 1.3 : 1
10% – 90% risetime	< 30 ns

CONCLUSION

An L-band monolithic FET switch has been demonstrated. By placing DC blocking capacitors in the source of the shunt FETs the switch became significantly less sensitive to DC bias ripple than conventional switch topologies. A 1.2 1 VSWR in the off state was achieved by taking advantage of the on channel resistance of the first shunt FETs. The switch uses only microamperes of current and is compatible with TTL or CMOS logic levels.